UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/062,620	01/31/2002	Srikanth R. Muroor	01-B-082 (STMI01-01082)	2429

7590 05/05/2005

Lisa K. Jorgenson, Esq.
STMicroelectronics, Inc.
1310 Electronics Drive
Carrollton, TX 75006

EXAMINER	
AMIN, NIRAV S	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/062,620	MUROOR, SRIKANTH R.	
	Examiner	Art Unit	
	Nirav S. Amin	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 are pending in the application.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Boutaud (USPN: 6,600,345).

As per claim 1, Boutad discloses:

a first clock control circuit that receives said first input clock signal and a first start signal, wherein said first start signal, when asserted, is capable of causing said first clock control circuit to output a first gated clock signal [Figure 4a, (442); Column 1, lines 58-64; Column 3, lines 36-41];

a second clock control circuit that receives said second input clock signal and a second start signal, wherein said second start signal, when asserted, is capable of causing said second clock control circuit to output a second gated clock signal [Figure 4a, (446); Column 1, lines 58-64; Column 3, lines 36-41];

a first interlock circuit that detects when said first clock control circuit begins outputting said first gated clock signal and, in response to said detection, that asserts a first disable signal capable of preventing said second clock control circuit from

outputting said second gated clock signal [Figure 4a, (406); Column 1, lines 49-53; Column 4, lines 19-20];

a second interlock circuit that detects when said second clock control circuit begins outputting said second gated clock signal and, in response to said detection, that asserts a second disable signal capable of preventing said first clock control circuit from outputting said first gated clock signal [Figure 4a, (408); Column 4, lines 26-28]; and

a first OR gate that receives said first and second gate clock signal and outputs said selected clock signal [Column 4, lines 4-10].

As per claim 11, Boutaud discloses:

a clocked circuit capable of operating at a plurality of clock frequencies [Figure 5a];

a first clock signal source [CLOCK_1];

a second clock signal source [CLOCK_2];

a clock selection circuit capable of receiving a first input clock signal from said first clock signal source and a second input clock signal from said second clock signal source and outputting to said clocked circuit a selected clock signal derived from one of said first and second input clock signals, said clock selection circuit comprising:

a first clock control circuit that receives said first input clock signal and a first start signal, wherein said first start signal, when asserted, is capable of causing said first clock control circuit to output a first gated clock signal [Figure 4a, (442); Column 1, lines 58-64; Column 3, lines 36-41];

a second clock control circuit that receives said second input clock signal and a second start signal, wherein said second start signal, when asserted, is capable of causing said second clock control circuit to output a second gated clock signal [Figure 4a, (446); Column 1, lines 58-64; Column 3, lines 36-41];

a first interlock circuit that detects when said first clock control circuit begins outputting said first gated clock signal and, in response to said detection, that asserts a first disable signal capable of preventing said second clock control circuit from outputting said second gated clock signal [Figure 4a, (406); Column 1, lines 49-53; Column 4, lines 19-20];

a second interlock circuit that detects when said second clock control circuit begins outputting said second gated clock signal and, in response to said detection, that asserts a second disable signal capable of preventing said first clock control circuit from outputting said first gated clock signal [Figure 4a, (408); Column 4, lines 26-28]; and

a first OR gate that receives said first and second gate clock signal and outputs said selected clock signal [Column 4, lines 4-10].

As per claims 3 and 13, Boutaud discloses:

a first clock enable circuit that receives said second disable signal and said first start signal and outputs a first clock enable signal when said first start signal is asserted and said second disable signal is not asserted [Figure 4a; Column 7, lines 48-53; SEL1 and EN2 are inputted into 408 and EN1 is outputted]; and

a first AND gate having a first input coupled to said first clock enable signal and a second input coupled to said first input clock signal, wherein said first AND gate outputs said first gated clock signal [Figure 4a, (442)].

As per claims 4 and 14, Boutaud discloses:

wherein said first clock enable circuit comprises a first input logic circuit having an output that outputs a Logic 1 when said first start signal is asserted and said second disable signal is not asserted [Figure 4a; Column 7, lines 48-53].

As per claims 5 and 15, Boutaud discloses:

a first flip-flop having an input coupled to said output of said first input logic circuit, wherein said first flip-flop is clocked by a rising edge of said first input clock signal and said first interlock circuit monitors an output of said first flip-flop to detect when said first clock control circuit begins outputting said first gated clock signal [Figure 4a].

As per claims 6 and 16, Boutaud discloses:

a second flip-flop having an input coupled to said output of said first flip flop, wherein said second flip-flop is clocked by a falling edge of said first input clock signal; and

a second OR gate having a first input coupled to said output of said first flip-flop and a second input coupled to an output of said second flip-flop, wherein an output of said second OR gate comprises said first clock enable signal [Figure 4a].

As per claims 8 and 18, Boutaud discloses:

a second clock enable circuit that receives said first disable signal and said second start signal and outputs a second clock enable signal when said second start signal is asserted and said first disable signal is not asserted [Figure 4a; Column 7, lines 48-55; SEL2 and EN1 are inputted into 408 and EN2 is outputted]; and

a second AND gate having a first input coupled to said second clock enable signal and a second input coupled to said second input clock signal, wherein said second AND gate outputs said second gated clock signal [Figure 4a, (446)].

As per claims 9 and 19, Boutaud discloses:

wherein said second clock enable circuit comprises a second input logic circuit having an output that outputs a Logic 1 when said second start signal is asserted and said first disable signal is not asserted [Figure 4a; Column 7, lines 48-53].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nirav S. Amin whose telephone number is (571) 272-3821. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NA

THOMAS
SUPERVISORY
TECHNOLOGY